## REMARKS

Claims 1-20 remain pending in the present application. Applicants respectfully request reconsideration of the application in view of the remarks appearing below.

**General Remarks**

The Final Office Action maintains the rejections from the First Office Action with respect to claims 1-20, stating that Applicants assert certain "limitations [that] are not recited in the rejected claims." Responding to the arguments provided in Applicants' Response to First Office Action ("prior Response"), the Final Office Action views Applicants' discussion of the limitations of claims 1 and 14 as incorrectly "interpret[ing the claims] in light of the specification [because] limitations from the specification are not read into the claims." Applicants respectfully disagree.

Applicants submit that the bodies of independent claims 1 and 14 include language that supports the limitations asserted by Applicants in their prior Response. By including the term "comprising" in connection with the shift register latch (which is, itself, positively recited in the body of each claim), claims 1 and 14 recite elements of the shift register latch that are essential components. (*see* M.P.E.P. 2111.03 which cites Genentech, Inc. v. Chiron Corp., 112 F.3d 495, 501 (Fed. Cir. 1997) "[c]omprising is a term of art used in claim language which means that the named elements are essential ..."). Referring to the Status of the Claims above, claim 1 recites in its body: "at least one shift register latch comprising: a first latch; a second latch ...; an input ...; and a circuit, connected between said input and said first latch, configured for generating a second clock signal ..." [Emphasis added]. With continued reference to the Status of the Claims, claim 14 recites in its body: "at least one shift register latch comprising: a first latch; a second

latch …; an input …; and a circuit, connected between said input and said first latch, configured for generating a second clock signal …" [Emphasis added]

As discussed in Applicants' prior Response, by including the term "comprising" in the body of claims 1 and 14, the claims "require that the shift register latch itself contain the second-clock-generating circuit between the input and the first latch." [Emphasis added.] Because each of these elements is explicitly recited in claims 1 and 14, it is unnecessary to read these limitations from the remainder of the specification. Accordingly, as suggested in Applicants' prior Response and elaborated in more detail below, these limitations (and others) distinguish claims 1 and 14, and claims 2-6 and 15-20 that depend therefrom, over the references of record.

Applicants further submit that the language utilized in the body of independent claim 7 give rise to similar explicit limitations as well. Referring once again to the Status of the Claims above, claim 7 recites "at least one shift register latch comprising: a master latch; a slave latch …; and a circuit element, electrically connected between said first clock and said master latch, adapted for generating a second clock signal …" [Emphasis added.] Because claim 7 explicitly recites several elements after the term "comprising," it is unnecessary to read these limitations from the remainder of the specification. Accordingly, as discussed in more detail below, these limitations (and others) distinguish claim 7, and claims 8-13 that depend therefrom, over the references of record.

**Rejection Under 35 U.S.C. § 102(b)**

Claims 1-2, 5-7, and 10-13 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,304,122 to Gregor et al., stating that Gregor et al. disclose all of the limitations of these claims. Applicants respectfully disagree.

Gregor et al. disclose a flip-flop device having fewer clock trees than prior devices and that supports Level Sensitive Scan Design (LSSD) functionality. In relevant part, Gregor et al.

disclose a shift register latch 1140 (FIGS. 11 and 15) that includes a master latch 1520 (FIG. 15) and a slave latch 1530 (FIG. 15). Gregor et al. further disclose a gate logic 140 (FIG. 2) that generates a single clock (e.g., an inverted C clock) from several inputs.

***Claims 1, 2, 3, 5, and 6***

In view of the foregoing General Remarks, Applicants respectfully submit that Gregor et al. do not disclose or suggest the subject matter of independent claim 1, nor claims 2, 3, 5, and 6 that depend therefrom. As discussed above, independent claim 1 requires in its body "at least one shift register latch comprising: ... an input for receiving a first clock signal; and a circuit, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal."

Applicants are unable to see the connection between the Single Clock of FIG. 11 and gating logic 140. Referring to Gregor et al. FIG. 11, a flushable single clock splitter system 1100 is illustrated in which a flushable single clock splitter 1130 provides two clock signals from a single clock signal (i.e., Single Clock). Not only is the Single Clock remote from the shift register latch 1140 of FIG. 11, but so is clock splitter 1130. Applicants assert that because Gregor et al. themselves designate the clock splitter 1130 as wholly separate and distinct from the shift register latch 1140, it is not reasonable in the art to say that the Gregor et al. Single Clock is a first clock signal received by an input of the shift register latch.

In addition, referring to Gregor et al. FIG. 2, it is readily seen that gating logic 140 "allows [an] inverted C clock to be created from the C clock, enable signal (EN) and edge (E) clock." Col. 6, par. 20-22. While this inverted C clock is received by master latch 120, it does not follow that gating logic 140 is "a circuit, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal." [Emphasis added]. Applicants also fail to see how Single Clock of FIG. 11, gating

logic 140 and the passage at col. 4, lines 20-25 support the Office Action's position that Gregor et al. teach a second-clock-generating circuit that compensates for a delay in a clock signal. Even if Single Clock (FIG. 11) was a "first input clock" (which is incorrect), neither FIG. 2, FIG. 11 nor the passage describe an element that can reasonably be considered "a circuit ... that compensates for any delay in [a] first clock signal," as recited by claim 1. Instead, while Gregor et al. are silent as to having a circuit that compensates for delay, Gregor et al. disclose gating logic 140 that "is used to generate a single clock (preferably an inverted C clock) from several inputs." Col. 4, lines 20-25. Thus, any reasonable interpretation of the underlined portion describes a circuit that inverts a clock signal, not a "circuit ... that compensates for any delay," as required by claim 1.

The U.S. Patent and Trademark Office (USPTO) is reminded that for an anticipation rejection to be proper, not only must every claim element be found in single reference, but the reference must also teach the exact arrangement of the claim elements as that arrangement is set forth in the claims. See MPEP § 2131. Applicants have not found even a suggestion in the Gregor et al. patent that any of the circuitry disclosed by Gregor et al. is intended to compensate for delay in a clock signal. Neither do Applicants see how Gregor et al. even suggests the arrangements of elements required by the present claims. Since the Gregor et al. patent does not appear to reasonably teach at least the delay compensation element of independent claim 1 and does not appear to reasonably teach the claimed arrangement of elements, Applicants believe it cannot anticipate this claim. If the USPTO continues this rejection, Applicants respectfully request that it explicitly point to where the Gregor et al. patent teaches compensating for clock delay.

Because the Gregor et al. patent does not include all of the limitations of independent claim 1, this claim and claims 2, 3, 5 and 6 that depend therefrom cannot be anticipated by the Gregor et al. patent.

In addition, regarding claims 5 and 6, Applicants fail to see how FIG. 13 and the passage at col. 8, lines 6-20 support the Office Action's position that Gregor et al. teach that the pulses of a second clock signal are shorter in duration than the pulses of a first clock signal. Although Gregor et al. disclose an L1 clock (FIG. 13) and an L2 clock (FIG. 13) that are delayed versions of a clock pulse (FIG. 13), the L1 clock and the L2 clock are illustrated in FIG. 13 as having the same duration as the clock pulse. Since neither FIG. 13 nor the passage describe pulses of a second clock signal that are shorter in duration than the pulses of a first clock signal, the Gregor et al. patent cannot anticipate claims 5 and 6.

Furthermore, claim 3 requires the circuit (which, again, is located between the input to the shift register latch and the first latch) to have a "pulse generator." The Office Action asserts that Gregor et al. disclose a pulse generator at the Single Clock in FIG. 11. As discussed above in relation to claim 1, Applicants assert that it is not reasonable in the art to say that the Gregor et al. Single Clock is part of the shift register latch. Because Gregor et al. designate the shift register latch as element 1140, which is wholly separate and distinct from the Single Clock, anyone of ordinary skill in the art would likewise make such a distinction.

In addition, using the Office Action's rational for rejecting claim 1, (which is incorrect) the Gregor et al. circuit corresponding to the compensating circuit of claim 1 is the clock splitter 1130 (FIG. 11). Clock splitter 1130 generates the clock signal for the master latch 1520 (FIG. 15) from the Single Clock. Consequently, the Single Clock is not the clock signal L1 Clock for master latch 1520. Claim 3, in contrast, requires that the pulse generator is "for generating a first

clock pulse for said first latch." [Emphasis added.] Any reasonable interpretation of the preceding underlined portion requires the pulse generator to be immediately upstream from the first latch, not at least once removed through clock splitter 1130. For this additional reason, the Gregor et al. patent cannot anticipate claim 3.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present rejection of claims 1, 2, 3, 5, and 6.

***Claims 7 and 10-13***

Referring to the General Remarks and the comments immediately above, Applicants respectfully submit that Gregor et al. do not disclose or suggest the subject matter of independent claim 7, nor claims 10-13 that depend therefrom.

As discussed above, claim 7 recites explicitly a limitation that is very similar in character to the limitation of claim 1 relative to the circuit that compensates for any delay in the first clock signal. In the case of independent claim 7, this claim requires a "circuit element adapted for generating a second clock signal that compensates for any delay in said first clock signal." [Emphasis added]. In the same manner that Gregor et al. fail to disclose or suggest a circuit having this compensation feature, Gregor et al. also fail to disclose or suggest a circuit element having this feature. Therefore, the Gregor et al. patent cannot anticipate claim 7, nor claims 10-13 that depend therefrom.

In addition, claim 12 requires, by its dependency from claims 7 and 11, that the integrated circuit include a plurality of shift register latches each having the unique timing-compensation circuit element of claim 7, as well as a plurality of shift register latches that do not have these timing-compensation circuit elements. Gregor et al. are silent on having two sets of shift register latches differing by the presence/absence of a timing-compensation circuit element. For this additional reason, the Gregor et al. patent cannot anticipate claim 12.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present rejection of claims 7 and 10-13.

**Rejection Under 35 U.S.C. § 103(a)**

Claims 4, 8, and 9-20 stand rejected under 35 U.S.C. § 103(a) as obvious in view of a combination of U.S. Patent Application No. 2004/0061539 to Joordens et al. and the Gregor et al. patent, discussed above.

The Joordens et al. patent discloses a clock recovery circuit to correct the timing relationship between a data signal and a clock signal. This circuit includes a phase detector that is "applicable to data and clock recovery at higher frequencies." Par. 007. This phase detector receives three input signals, e.g., "an input for receiving a clock signal, an input for receiving a data signal and an input for receiving a window signal." Abstract. The detector generates two outputs, an up and a down pulse, through the application of at least two separate AND gates, as illustrated in FIGS. 1, 3A, 4A, 7 and 8.

***Claim 4, 8, and 9***

The Office Action states that Gregor et al. disclose all the limitations of claims 4, 8, and 9 except "an AND gate and an inverter." The Office Action further states that Joordens et al. disclose these missing limitations and asserts that it would have been obvious to a person having ordinary skill in the art at the time of the invention to add this limitation to the Gregor et al. device. Applicants respectfully disagree.

First, neither Joordens et al. nor Gregor et al. disclose or suggest a pulse generator that generates and provides a clock pulse to a first latch of a shift register latch as required in claims 4, 8, and 9. Joorden et al. are silent on such a pulse generator, since there is no shift register latch involved in their patent. Likewise, as discussed relative to claim 3 above, Gregor et al. disclose a Single Clock (FIG. 15) that cannot reasonably be considered a "pulse generator" by

those skilled in the art. Moreover, in FIG. 12, Gregor et al. disclose a flushable single clock splitter 1130. Although clock splitter 1130 generates the L1 clock and the L2 clock, it is readily seen in stark contrast that the clock splitter 1130 that is asserted to be within the shift register latch is in fact a component external to the shift register latch.

Second, even though Joordens et al. show AND gates, none of these gates is used for the purposes recited in claims 4, 8 and 9. Instead, Joordens et al. disclose AND gates that are part of a phase detector circuit for "detect[ing the] rising edges of [a] data and clock." Par. 0044.

Third, Applicants fail to see any reasons to combine the elements of the Joordens et al. and Gregor et al. patents in the fashion recited by claims 4, 8 and 9. The Office Action does not set forth any assertion specific to shift register latches to which the present invention is directed. Instead, the Office Action generally states that "one of ordinary skill in the art would have found it obvious to use the phase detector of Joordens et al. to acquire distorted signals at very high data rates and to provide clock signal and retimed or recovered data as outputs," a statement that does not constitute a *prima facie* showing of obviousness. Applicants respectfully assert that the U.S. Patent and Trademark Office must make a more problem-specific argument to satisfy the *prima facie* case requirement of MPEP § 2143.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present rejection of claims 4, 8 and 9.

***Claims 14-20***

Regarding claims 14 and 15, the Office Action states that Gregor et al. disclose the limitations of these claims except "a power supply connected to the integrated circuit." The Office Action then states that Joordens et al. disclose this missing limitation and asserts that it would have been obvious to a person having ordinary skill in the art at the time of the invention to add this limitation to the Joordens et al. apparatus. Applicants respectfully disagree.

Independent claim 14, like independent claim 1 discussed above, requires a "circuit, connected between said input and said first latch, configured for generating a second clock signal that compensates for any delay in said first clock signal." [Emphasis added.] As discussed above relative to claim 1, Gregor et al. simply do not disclose or suggest this limitation. Joordens et al. obviously do not disclose or suggest this limitation since the subject matter of their patent is vastly different. Since neither of the patents disclose or suggest this limitation, neither independent claim 14, nor claims 15-20 that depend therefrom, is obvious in view of the combination.

In addition, each of claims 16-18 includes a limitation that corresponds to a limitation in corresponding respective ones of claims 3-5. As discussed above, Gregor et al. do not disclose or suggest these limitations. Joordens et al. do not disclose these limitations, either. Therefore, claims 16-18 are not obvious in view of the combination of the Gregor et al. and Joordens et al. patents for this additional reason.

For at least the foregoing reasons, Applicants respectfully request that the Examiner withdraw the present rejection.

## CONCLUSION

In view of the foregoing, Applicants submit that claims 1-20 are in condition for allowance. Therefore, prompt issuance of a Notice of Allowance is respectfully solicited. If any issues remain, the Examiner is encouraged to call the undersigned attorney at the number listed below.

Respectfully submitted,

INTERNATIONAL BUSINESS MACHINES CORP.

By:_____

Michael J. Wasco
Registration No.: 58,919
DOWNS RACHLIN MARTIN PLLC
Tel: (802) 863-2375
Attorneys for Assignee

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